CLAIMS

1. A delay-locked loop, comprising:

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to the ring oscillator and operable to generate a coarse delay count responsive to the oscillator clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to the coarse delay reference count, and the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a fine delay control signal to select one of the tap clock signals and output the selected signal as a fine delay enable signal;

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count; and

a comparison circuit adapted to receive an input clock signal and coupled to the output circuit to receive the delayed clock signal, and the comparison circuit being further coupled to the coarse and fine delay circuits, the comparison circuit operable to generate the coarse and fine delay control signals in response to the relative phases of the delayed and input clock signals.

2. The delay-locked loop of claim 1 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the comparison circuit determines a phase

difference between the delayed and input clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less than NxTPD, and thereafter generates the fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference less than or equal to TPD.

3. The delay-locked loop of claim 1 wherein the coarse delay circuit comprises:

a coarse reference counter coupled to the comparison circuit and operable to develop a coarse reference count responsive to the coarse delay control signal;

a coarse delay counter coupled to the ring oscillator to receive the oscillator clock signal and coupled to output circuit to receive the delayed clock signal, the coarse delay counter developing a coarse delay count responsive to the oscillator clock signal and resetting the coarse delay count responsive to the delayed clock signal; and

a comparator circuit coupled to the coarse reference and delay counters, the comparator circuit activating the coarse delay enable signal responsive to the coarse delay count being equal to the coarse reference count.

4. The delay-locked loop of claim 1 wherein the fine delay circuit comprises:

a plurality of transmission gates, each transmission gate including a first signal terminal coupled to the ring oscillator to receive a respective tap clock signal, a second signal terminal coupled to the output circuit, and a control terminal that receives a fine delay selection signal, each transmission gate coupling the first signal terminal to the second signal terminal in response to the fine delay selection signal being activated; and

a shift register coupled to the comparison circuit to receive the fine delay control signal and having a plurality of stages, each stage being coupled to the control terminal of a respective transmission gate, the shift register operable responsive to the fine delay control signal to shift an active bit into a selected one of the stages, the active bit activating the

corresponding fine delay selection signal to apply the corresponding tap signal as the fine delay enable signal to the output circuit.

5. The delay-locked loop of claim 1 wherein the output circuit comprises an AND gate.

6. The delay-locked loop of claim 1 wherein the comparison circuit comprises:

a feedback delay line that generates a feedback clock signal in response to the delayed clock signal, the feedback clock signal having a feedback delay relative to the delayed clock signal; and

a phase detector coupled to receive the feedback clock signal and the input clock signal, and operable to generate the coarse and fine delay control signals responsive to a detected phase between the feedback and input clock signals.

7. The delay-locked loop of claim 6 wherein the phase detector detects the phase between rising-edges of the feedback and input clock signals.

8. The delay-locked loop of claim 6 wherein the feedback delay comprises a first delay and a second delay, the first delay including a delay of an input buffer adapted to receive an external clock signal an develop the input clock signal in response to the external clock signal, and the second delay including a delay of the output circuit and a delay of an output buffer that receives the delayed clock signal and generates a synchronized clock signal in response to the delayed clock signal.

9. A delay-locked loop, comprising:

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to the ring oscillator and operable to generate a coarse delay count responsive to the oscillator clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to the coarse delay reference count, and the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a rising-edge fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a rising-edge fine delay control signal to select one of the tap clock signals and output the selected signal as a rising-edge fine delay enable signal;

a falling-edge fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a falling-edge fine delay control signal to select one of the tap clock signals and output the selected signal as a falling-edge fine delay enable signal;

an output circuit coupled to the coarse, rising-edge, and falling-edge delay circuits, the output circuit generating a rising-edge of a delayed clock signal responsive to the coarse and rising-edge fine delay enable signals going active, and the output circuit generating a falling-edge of the delayed clock signal responsive to the coarse and falling-edge fine delay enable signals going active, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count responsive to each transition of the delayed clock signal; and

a comparison circuit adapted to receive an input clock signal and coupled to the output circuit to receive the delayed clock signal, and the comparison circuit being further coupled to the coarse and fine delay circuits, the comparison circuit operable to generate the coarse and rising-edge and falling-edge fine delay control signals in response to the relative phases of the rising-edges and falling-edges of the delayed and input clock signals.

10. The delay-locked loop of claim 9 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the comparison circuit determines a phase difference between the rising and falling edges of the delayed and input clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less than NxTPD, and thereafter generates the rising-edge and falling-edge fine delay control signals to select respective tap clock signals, each selected tap signal making the corresponding phase difference less than or equal to TPD.

11. The delay-locked loop of claim 9 wherein the coarse delay circuit comprises:

a coarse reference counter coupled to the comparison circuit and operable to develop a coarse reference count responsive to the coarse delay control signal;

a coarse delay counter coupled to the ring oscillator to receive the oscillator clock signal and coupled to output circuit to receive the delayed clock signal, the coarse delay counter developing a coarse delay count responsive to the oscillator clock signal and resetting the coarse delay count responsive to the delayed clock signal; and

a comparator circuit coupled to the coarse reference and delay counters, the comparator circuit activating the coarse delay enable signal responsive to the coarse delay count being equal to the coarse reference count.

12. The delay-locked loop of claim 9 wherein each of the fine delay circuits comprises:

a plurality of transmission gates, each transmission gate including a first signal terminal coupled to the ring oscillator to receive a respective tap clock signal, a second signal terminal coupled to the output circuit, and a control terminal that receives a fine delay

selection signal, each transmission gate coupling the first signal terminal to the second signal terminal in response to the fine delay selection signal being activated; and

a shift register coupled to the comparison circuit to receive the fine delay control signal and having a plurality of stages, each stage being coupled to the control terminal of a respective transmission gate, the shift register operable responsive to the fine delay control signal to shift an active bit into a selected one of the stages, the active bit activating the corresponding fine delay selection signal to apply the corresponding tap signal as the fine delay enable signal to the output circuit.

13. The delay-locked loop of claim 9 wherein the output circuit comprises:

a first AND gate coupled to receive the coarse delay enable signal and the rising-edge fine delay enable signal on respective inputs, and operable to develop a rising-edge enable signal on an output;

a second AND gate coupled to receive the coarse delay enable signal and the falling-edge fine delay enable signal on respective inputs, and operable to develop a falling-edge enable signal on an output; and

a set-reset flip-flop having a set input coupled the first AND gate and having a reset input coupled to the second AND gate, the flip-flop generating a rising-edge of the delayed clock signal on an output responsive to the set input and generating a falling-edge of the delayed-clock signal responsive to the reset input.

14. The delay-locked loop of claim 9 wherein the comparison circuit comprises:

a feedback delay line that generates a feedback clock signal in response to the delayed clock signal, the feedback clock signal having a feedback delay relative to the delayed clock signal;

a rising-edge phase detector coupled to receive the feedback clock signal and the input clock signal, and operable to generate the coarse and rising-edge fine delay control

signals responsive to a detected phase between rising-edges of the feedback and input clock signals; and

a falling-edge phase detector coupled to receive the feedback clock signal and the input clock signal, and operable to generate the coarse and falling-edge fine delay control signals responsive to a detected phase between falling-edges of the feedback and input clock signals.

15. The delay-locked loop of claim 14 wherein the rising-edge and falling-edge phase detectors receive the input clock signal and a complementary input clock signal, respectively.

16. The delay-locked loop of claim 14 wherein the feedback delay comprises a first delay and a second delay, the first delay including a delay of an input buffer adapted to receive an external clock signal an develop the input clock signal in response to the external clock signal, and the second delay including a delay of the output circuit and a delay of an output buffer that receives the delayed clock signal and generates a synchronized clock signal in response to the delayed clock signal.

17. A delay-locked loop, comprising:

an input buffer circuit adapted to receive an input clock signal and operable to generate a buffered clock signal in response to the input clock signal;

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to the ring oscillator and operable to generate a coarse delay count responsive to the oscillator clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to

the coarse delay reference count, and the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a fine delay control signal to select one of the tap clock signals and output the selected signal as a fine delay enable signal;

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count; and

a feedback delay line coupled to the output circuit and operable to generate a feedback clock signal in response to the delayed clock signal, the feedback clock signal having a feedback delay relative to the delayed clock signal;

a phase detector coupled to the feedback delay line, input buffer, coarse delay circuit, and fine delay circuit, and operable to generate the coarse and fine delay control signals responsive to a detected phase between the buffered and feedback clock signals; and

an output buffer coupled to the output circuit and operable to generate a synchronized clock signal in response to the delayed clock signal.

18. The delay-locked loop of claim 17 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the phase detector determines a phase difference between the buffered and feedback clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less than NxTPD, and thereafter generates the fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference less than or equal to TPD.

19. The delay-locked loop of claim 17 wherein the coarse delay circuit comprises:

a coarse reference counter coupled to the phase detector and operable to develop a coarse reference count responsive to the coarse delay control signal;

a coarse delay counter coupled to the ring oscillator to receive the oscillator clock signal and coupled to output circuit to receive the delayed clock signal, the coarse delay counter developing a coarse delay count responsive to the oscillator clock signal and resetting the coarse delay count responsive to the delayed clock signal; and

a comparator circuit coupled to the coarse reference and coarse delay counters, the comparator circuit activating the coarse delay enable signal responsive to the coarse delay count being equal to the coarse reference count.

20. The delay-locked loop of claim 17 wherein the fine delay circuit comprises:

a plurality of transmission gates, each transmission gate including a first signal terminal coupled to the ring oscillator to receive a respective tap clock signal, a second signal terminal coupled to the output circuit, and a control terminal that receives a fine delay selection signal, each transmission gate coupling the first signal terminal to the second signal terminal in response to the fine delay selection signal being activated; and

a shift register coupled to the comparison circuit to receive the fine delay control signal and having a plurality of stages, each stage being coupled to the control terminal of a respective transmission gate, the shift register operable responsive to the fine delay control signal to shift an active bit into a selected one of the stages, the active bit activating the corresponding fine delay selection signal to apply the corresponding tap signal as the fine delay enable signal to the output circuit.

21. The delay-locked loop of claim 17 wherein the output circuit comprises an AND gate.

22. The delay-locked loop of claim 17 wherein the phase detector detects the phase between rising-edges of the feedback and input clock signals.

23. The delay-locked loop of claim 17 wherein the feedback delay comprises a first delay component and a second delay component, the first delay component corresponding to a delay of the input buffer and the second delay component corresponding to a delay of the output buffer.

24. A delay-locked loop, comprising:

an input buffer circuit adapted to receive an input clock signal and operable to generate a buffered clock signal in response to the input clock signal;

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to the ring oscillator and operable to generate a coarse delay count responsive to the oscillator clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to the coarse delay reference count, and the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a rising-edge fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a rising-edge fine delay control signal to select one of the tap clock signals and output the selected signal as a rising-edge fine delay enable signal;

a falling-edge fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a falling-edge fine delay control signal to select one of the tap clock signals and output the selected signal as a falling-edge fine delay enable signal;

an output circuit coupled to the coarse, rising-edge, and falling-edge delay circuits, the output circuit generating a rising-edge of a delayed clock signal responsive to the

coarse and rising-edge fine delay enable signals going active, and the output circuit generating a falling-edge of the delayed clock signal responsive to the coarse and falling-edge fine delay enable signals going active, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count responsive to each transition of the delayed clock signal;

a feedback delay line coupled to the output circuit and operable to generate a feedback clock signal in response to the delayed clock signal, the feedback clock signal having a feedback delay relative to the delayed clock signal;

a phase detector coupled to the feedback delay line, input buffer, coarse delay circuit, and fine delay circuits, and operable to generate the coarse delay control signal and the rising-edge delay control signal responsive to a detected phase between rising-edges of the buffered and feedback clock signals, and operable to generate the coarse delay control signal and the falling-edge delay control signal responsive to a detected phase between the falling-edges of the buffered and feedback clock signals; and

an output buffer coupled to the output circuit and operable to generate a synchronized clock signal in response to the delayed clock signal.

25. The delay-locked loop of claim 24 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the phase detector determines a phase difference between the rising-edges of the buffered and feedback clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD and until the determined phase difference is less than NxTPD, and generates the rising-edge fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference between rising-edges less than or equal to TPD, and generates the falling-edge fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference between falling-edges less than or equal to TPD.

26. The delay-locked loop of claim 24 wherein the coarse delay circuit comprises:

a coarse reference counter coupled to the phase detector and operable to develop a coarse reference count responsive to the coarse delay control signal;

a coarse delay counter coupled to the ring oscillator to receive the oscillator clock signal and coupled to output circuit to receive the delayed clock signal, the coarse delay counter developing a coarse delay count responsive to the oscillator clock signal and resetting the coarse delay count responsive to each transition of the delayed clock signal; and

a comparator circuit coupled to the coarse reference and delay counters, the comparator circuit activating the coarse delay enable signal responsive to the coarse delay count being equal to the coarse reference count.

27. The delay-locked loop of claim 24 wherein each fine delay circuit comprises:

a plurality of transmission gates, each transmission gate including a first signal terminal coupled to the ring oscillator to receive a respective tap clock signal, a second signal terminal coupled to the output circuit, and a control terminal that receives a fine delay selection signal, each transmission gate coupling the first signal terminal to the second signal terminal in response to the fine delay selection signal being activated; and

a shift register coupled to the phase detector to receive the fine delay control signal and having a plurality of stages, each stage being coupled to the control terminal of a respective transmission gate, the shift register operable responsive to the fine delay control signal to shift an active bit into a selected one of the stages, the active bit activating the corresponding fine delay selection signal to apply the corresponding tap signal as the fine delay enable signal to the output circuit.

28. The delay-locked loop of claim 24 wherein the output circuit comprises:

a first AND gate coupled to receive the coarse delay enable signal and the rising-edge fine delay enable signal on respective inputs, and operable to develop a rising-edge enable signal on an output;

a second AND gate coupled to receive the coarse delay enable signal and the falling-edge fine delay enable signal on respective inputs, and operable to develop a falling-edge enable signal on an output; and

a set-reset flip-flop having a set input coupled the first AND gate and having a reset input coupled to the second AND gate, the flip-flop generating a rising-edge of the delayed clock signal on an output responsive to the rising-edge enable signal on the set input and generating a falling-edge of the delayed-clock signal responsive to the falling-edge enable signal on the reset input.

29. The delay-locked loop of claim 9 wherein the phase detector comprises:

a rising-edge phase detector coupled to receive the feedback clock signal and the buffered clock signal, and operable to generate the coarse delay control signal and rising-edge fine delay control signal responsive to a detected phase between rising-edges of the feedback and buffered clock signals; and

a falling-edge phase detector coupled to receive the feedback clock signal and the buffered clock signal, and operable to generate the coarse delay control signal and falling-edge fine delay control signal responsive to a detected phase between falling-edges of the feedback and buffered clock signals.

30. The delay-locked loop of claim 29 wherein the input buffer comprises:

a first input buffer adapted to receive a true input clock signal and operable to apply a true buffered clock signal to the rising-edge phase detector responsive to the true input clock signal; and

a second input buffer adapted to receive a complementary input clock signal and operable to apply a complementary buffered clock signal to the falling-edge phase detector responsive to the complementary input clock signal.

31. The delay-locked loop of claim 24 wherein the feedback delay comprises a first delay and a second delay, the first delay including a delay of the input buffer and the second delay including a delay of the output circuit.

32. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a delay-locked loop coupled to at least the control circuit and adapted to receive an input clock signal, the delay-locked loop operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the delay-locked loop comprising,

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to the ring oscillator and operable to generate a coarse delay count responsive to the oscillator clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to

the coarse delay reference count, and the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a fine delay control signal to select one of the tap clock signals and output the selected signal as a fine delay enable signal;

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count; and

a comparison circuit adapted to receive the input clock signal and coupled to the output circuit to receive the delayed clock signal, and the comparison circuit being further coupled to the coarse and fine delay circuits, the comparison circuit operable to generate the coarse and fine delay control signals in response to the relative phases of the delayed and input clock signals.

33. The memory device of claim 32 wherein the memory device comprises a DDR SDRAM and the delay-locked loop receives complementary input clock signals and generates the delayed clock signal that is synchronized to the rising and falling edges of the clock signals, the delayed clock signal being applied to clock an output driver coupled to the data bus.

34. The memory device of claim 32 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the comparison circuit determines a phase difference between the delayed and input clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less than NxTPD, and thereafter generates the fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference less than or equal to TPD.

35. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a delay-locked loop coupled to at least the control circuit and adapted to receive an input clock signal, the delay-locked loop operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the delay-locked loop comprising,

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal, each clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to the ring oscillator and operable to generate a coarse delay count responsive to the oscillator clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to the coarse delay reference count, and the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a fine delay control signal to select one of the tap clock signals and output the selected signal as a fine delay enable signal;

an output circuit coupled to the coarse and fine delay circuits, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals going active, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count; and

a comparison circuit adapted to receive the input clock signal and coupled to the output circuit to receive the delayed clock signal, and the comparison circuit being further coupled to the coarse and fine delay circuits, the comparison circuit operable to generate the coarse and fine delay control signals in response to the relative phases of the delayed and input clock signals.

36. The computer system of claim 35 wherein the memory device comprises a DDR SDRAM and the delay-locked loop receives complementary input clock signals and generates the delayed clock signal that is synchronized to the rising and falling edges of the clock signals, the delayed clock signal being applied to clock an output driver coupled to the data bus.

37. The computer system of claim 32 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the comparison circuit determines a phase difference between the delayed and input clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less than NxTPD, and thereafter generates the fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference less than or equal to TPD.

38. A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of oscillator clock signals, each oscillator clock signal having a frequency that is greater than the applied clock signal, with one oscillator clock signal being designated a reference oscillator clock signal and each oscillator clock signal having a delay relative to the reference oscillator clock signal;

detecting a phase difference between the applied clock signal and the delayed clock signal;

generating a coarse reference count in response to the detected phase difference;

incrementing a coarse delay count responsive to the reference oscillator clock signal;

determining a coarse delay time when the coarse reference count equals the coarse delay count;

selecting one of the oscillator clock signals in response to the detected phase difference between the applied and delayed clock signals;

determining a fine delay time from the selected oscillator clock signal;

generating the delayed clock signal having a delay relative to the applied clock signal that equals the sum of the coarse and fine delay times; and

repeating the operations of detecting a phase difference between the applied clock signal and the delayed clock signal through generating the delayed clock signal having a delay relative to the applied clock signal that equals the sum of the coarse and fine delay times until the delayed clock signal has a locked delay relative to the applied clock signal.

39. The method of claim 38 wherein detecting a phase difference between the applied clock signal and the delayed clock signal comprises delaying the delayed clock signal by a model delay to generate a feedback clock signal, and detecting the phase difference between the feedback clock signal and the applied clock signal.

40. The method of claim 38 wherein the locked value corresponds to the applied clock signal being delayed relative to the delayed clock signal by an output buffer delay time.

41. The method of claim 38 further comprising clocking data in response to the delayed clock signal.

42. A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of oscillator clock signals, each oscillator clock signal having a frequency that is greater than the applied clock signal, with one oscillator clock signal being designated a reference oscillator clock signal and each oscillator clock signal having a delay relative to the reference oscillator clock signal;

detecting a phase difference between rising-edges of the applied and delayed clock signals;

detecting a phase difference between falling-edges of the applied and delayed clock signals;

generating a coarse reference count in response to the detected phase difference;

incrementing a coarse delay count responsive to the reference oscillator clock signal;

determining a coarse delay time when the coarse reference count equals the coarse delay count;

selecting one of the oscillator clock signals in response to the detected phase difference between the rising-edges of the applied and delayed clock signals;

determining a rising-edge fine delay time from the selected oscillator clock signal;

generating a rising-edge of the delayed clock signal having a delay relative to the applied clock signal that equals the sum of the coarse delay time and the rising-edge fine delay time;

selecting one of the oscillator clock signals in response to the detected phase difference between the falling-edges of the applied and delayed clock signals;

determining a falling-edge fine delay time from the selected oscillator clock signal;

generating a falling-edge of the delayed clock signal having a delay relative to the applied clock signal that equals the sum of the coarse delay time and the falling-edge fine delay time; and

repeating the operations of detecting a phase difference between rising-edges through generating a falling-edge of the delayed clock signal until the delayed clock signal has a locked delay relative to the applied clock signal.

43. The method of claim 42 wherein the applied clock signal comprises a true applied clock signal and a complementary applied clock signal, and wherein detecting a phase difference between rising-edges of the applied clock signal and the delayed clock signal comprises delaying the delayed clock signal by a model delay to generate a feedback clock signal and detecting the phase difference between rising-edges of the feedback and the true applied clock signals, and wherein detecting a phase difference between falling-edges the applied clock signal and the delayed clock signal comprises detecting the phase difference between a rising-edge of the complementary applied clock signal and a falling-edge of the feedback clock signal.

44. The method of claim 42 wherein the locked value corresponds to the applied clock signal being delayed relative to the delayed clock signal by an output buffer delay time.

45. The method of claim 42 further comprising clocking data in response to the delayed clock signal.